IN THE CLAIMS

Please substitute the following claims for the pending claims with the same numbers respectively:

Claims 1-11 (Cancelled):

Claim 12 (Previously presented): A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing;

a memory controller which is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses and controls erasing, writing, and reading of data; and

a host information memory which temporarily stores a write speed mode given by said access unit, wherein

said memory controller includes a nonvolatile memory access section which performs writing with respect to said plurality of nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on a speed mode stored in said host information memory.

Claim 13 (Previously presented): The semiconductor memory card according to claim 12, wherein said memory controller performs, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and sequentially performs writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a low speed mode.

Claim 14 (Previously presented): A semiconductor memory control apparatus used by being connected to a nonvolatile memory which includes a plurality of nonvolatile memory chips in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

a memory controller which is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses and controls erasing, writing, and reading of data; and

a host information memory which temporarily stores a write speed mode given by said access unit, wherein

said memory controller includes a nonvolatile memory access section which performs writing with respect to said plurality of nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on the speed mode stored in said host information memory.

Claim 15 (Previously presented): The semiconductor memory control apparatus according to claim 14, wherein said memory controller performs, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and sequentially performs writing with respect to said plurality of

nonvolatile memory chips when the write speed mode stored in said host information memory is at a low speed mode.

Claim 16 (Previously presented): A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing and a host information memory for temporarily storing a write speed mode given by an access unit, said semiconductor memory control method comprising the step of:

performing writing with respect to said plurality of nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on the speed mode stored in said host information memory.

Claim 17 (Previously presented): The semiconductor memory control method according to claim 16, further comprising the steps of:

performing, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and

sequentially performing writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a low speed mode.

Claims 18-23 (Cancelled):